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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,739	11/16/2001	David H. Harris	5087-27	3310

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EXAMINER	
DANG, KHANH NMN	
ART UNIT	**PAPER NUMBER**
2111	7

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/990,739	HARRIS ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The Declaration filed on 1/14/2003 under 37 CFR 1.131 is defective because of the following reasons.

The purpose of a 37 CFR 1.131 affidavit or declaration is to overcome a prior art rejection by proving invention of the claimed subject matter by applicant prior to the effective date of the reference relied upon in the rejection. The filing of this Declaration (1/14/2003) is prior to a First Office Action; wherein a rejection using a prior art reference involves. Therefore, this Declaration is defective.

Further, the Declaration alleged that "a universal serial bus (USB) interface for mass storage device as described and claimed in the application" was conceived and developed before October 5, 2000. However, the declaration does not include facts showing a completion of the invention prior to October 5, 2000. The exhibit "A" shows only a Product Data Sheet of bridge chip (ISD-300 ASIC). Further, there's no indication/evidence from the document showing Applicant's involvement with the product. Still further, there is no specific date on the document. As a matter of fact, a close examination of the ISD-300 ASIC Product Data Sheet (Revision 0.8), page 5, submitted by the Applicant, reveals that the actual dates ("Copyright" date and Document Revision History") of this document have been intentionally made blank. However, a copy of ISD-300 ASIC Product Data Sheet available to this Office clearly shows January 16, 2001 is the "Creation Time/Date" of Revision 0.8.

The Declaration alleged that "I and the other named inventors of U.S. Patent Application Serial No. 09/990,739 ("the application") conceived of and developed a universal serial bus (USB) interface for mass storage device as described and claimed in the application." However, the Declaration was signed on 8/1/2003 by only David H. Harris.

The Applicant is again reminded of Section 1001 of Title 18 of the United States Code, and of the fact that willful false statements may jeopardize the validity of the application of any patent issuing thereon.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Jacobs.

At the outset, it is noted that similar claims will be grouped together to avoid repetition.

As broadly drafted, these claims do not define any structure/step that differs from Jacobs.

With regard to claim 1, Jacobs discloses a method of communicating with a mass storage device, comprising: receiving ATA/ATAPI signals from a mass storage device (140) into a bridging circuit (156); converting the ATA/ATAPI signals from the mass storage device (140) into USB signals using the bridging circuit (156); and outputting the USB signals from the bridging circuit (156).

With regard to claim 2, in Jacobs, the bridging circuit (156) can be provided in a single IC.

With regard to claim 3, the bridging circuit (156) is provided on a motherboard of the mass storage device (see Fig. 6 and description thereof).

With regard to claim 4, the bridging circuit (156) is provided on a secondary board (physical device 160, see Figs. 7 and 8, and description thereof).

With regard to claim 5, the mass storage device (186) motherboard outputs ATA/ATAPI signals, and wherein the secondary board (of physical device 160) receives the ATA/ATAPI signals from the mass storage device (186) motherboard and converts them into USB signals (to host 130).

With regard to claim 6, Jacobs discloses a motherboard for a mass storage device (160), said motherboard comprising: input logic (ATA logic) configured to receive an input signal from a read unit of the mass storage device (160); a bridging circuit (156, Fig. 6) configured to receive the input signal from the input logic and convert the input

signal into a USB signal; and output circuitry configured to output the USB signal from the motherboard (of the ATA device 160).

With regard to claim 7, the bridging circuit (156) comprises a bridging chip (IC) for converting the input signal into the USB signal.

With regard to claim 8, the bridging chip (156) comprises: an ATA/ATAPI interface (ATA interface interfacing ATA device) configured to receive ATA/ATAPI signals from the input logic; a disk interface (of ATA disk interface) configured to receive ATA/ATAPI signals from the ATA/ATAPI interface; a serial interface engine (USB interface interfacing the host 130); and a USB physical interface transceiver (USB protocol requires USB physical interface transceiver to be in full compliance with USB specification) configured to receive signals from the serial interface engine and output USB signals to a USB interface (of host 130).

With regard to claim 9, Jacobs discloses a secondary board (of physical device 160) configured to enable communication between a mass storage device (186) motherboard and a host motherboard (of host 130), said secondary board comprising: a connector port (it is clear that connecting port is used to connect the secondary board to ATA device 186) for receiving signals from the mass storage device (186) motherboard; a bridging circuit (156) for converting signals from the mass storage device (186) motherboard into USB signals; and a USB connector port (USB port for connecting 160 to host 130) for outputting the USB signals to the host (130) motherboard. See also Figs. 7 and 8 and description thereof.

With regard to claim 10, the bridging circuit (156) comprises a bridging chip (IC) configured to translate the signals from the mass storage device motherboard into USB signals.

With regard to claim 11, the bridging chip (IC 156) comprises a USB physical interface transceiver (USB protocol requires USB physical interface transceiver to be in full compliance with USB specification), a serial interface engine (USB interface), and a disk interface (ATA disk interface).

With regard to claim 12, the disk interface receives ATA/ATAPI signals through an ATA/ATAPI interface, and wherein the ATA/ATAPI signals are converted into USB 2.0 signals (USB 2.0 is also employed in Jacobs) and are output to a USB Interface through the USB physical interface transceiver.

With regard to claim 13, Jacobs discloses a bridging chip (IC 156) comprising: an input configured to receive ATA/ATAPI signals; conversion logic configured to convert the ATA/ATAPI signals into USB signals; and an output configured to output the USB signals. See explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

With regard to claim 14, the input comprises an ATA/ATAPI interface arranged to receive the ATA/ATAPI signals and a disk interface configured to receive ATA/ATAPI signals from the ATA/ATAPI interface; wherein said conversion logic comprises a serial interface engine and a USB physical interface transceiver, said interface transceiver being configured to receive signals from the serial interface engine and output USB

signals to a USB interface. See explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

With regard to claim 15, the chip is located on a mass storage device motherboard. See explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

With regard to claim 16, the chip is located on a secondary board. See explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

With regard to claim 17, the secondary board is arranged to receive ATA/ATAPI signals from a motherboard of the mass storage device. See explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

With regard to claim 18, Jacobs discloses a method of converting signals from a mass storage device into USB signals, said method comprising: receiving a signal from a mass storage device into a bridging chip; converting the signal from the mass storage device into a USB signal; outputting the USB signal from the bridging chip. See explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

With regard to claim 19, the bridging chip is located on a motherboard of the mass storage device. See explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

With regard to claim 20, the bridging chip is located on a secondary board arranged in communication with a motherboard of the mass storage device. See

explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

U.S. Patent Nos. 6,292,863 to Terasaki et al., 6,633,933 to Smith et al., and 6,233,640 to Luke et al. are of particular interest and cited as relevant art. Terasaki et al., Smith et al., or Luke et al. disclose an apparatus and method for communication between an ATA mass storage device and a USB Host, comprising an ATA mass storage device; a USB Host; and a bridge for communication between the ATA device and the Host and for converting ATA protocol to USB protocol and vise versa.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner